Structure

PG CURRICULUM

For

M Tech. ES VLSI

w.e.f. Academic Year 2018-19

SHRI GURU GOBIND SINGHJI INSTITUTE OF ENGINEERING AND TECHNOLOGY, NANDED-431606, INDIA.

(An Autonomous Institute affiliated to SRTMU, Nanded)

Department of Electronics and Telecommunication

M. Tech. ES VLSI

Semester I

Sr. No	Course Type / code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 1 (PCC-EV-501)	Semiconductor Devices	3	0	0	3
2	Core 2 (PCC-EV-502)	Real Time Embedded Systems	3	0	2	4
3	Core 3 (PCC-EV-503)	Digital IC Design	3	0	2	4
4	Program specific elective – any two (PEC-EV-5AA)	Program Specific Elective 1 and 2 (Choose any two from the list) 504 Modern Digital Design using Verilog 505 Digital Signal and Image Processing 506 Object Oriented Programming 507 Computer Architecture 508 High Speed Digital Design 509 CAD of Digital System 510 IC Technology 511 Parallel Processing 512 Programmable Digital Signal Processors	3+3	0	2+2	4+4
5	Mandatory Credit (MCC-590)	Research Methodology and IPR	2	0	0	2
6	Mandatory Audit (MAC-591)	English for Research Paper Writing	2	0	0	-
					Total	21

Semester II

Sr. No	Course Type / code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Core 4 (PCC-EV-513)	Analog and Mixed Signal VLSI Design	3	0	2	4
2	Core 5 (PCC-EV-514)	Advanced Verification Techniques using System Verilog	3	0	2	4
3	Program specific elective – any one (PEC-EV-5BB)	Program Specific Elective 3 (VLSI)(Choose any one from the list) 515 Low Power VLSI Design 516 Memory Technologies 517 Physical Design Automation 518 Testability of VLSI Circuits 519 VLSI Signal Processing 520 SoC Design	3	0	2	4
4	Program specific elective – any one (PEC-EV-5CC)	Program Specific Elective 4 (ES)(Choose any one from the list) 521 Embedded Networking 522 System Design with Embedded OS 523 Communication Buses and Interfaces 524 Network Security and Cryptography	3	0	2	4
5	Open elective (OEC-8AA)	Open Elective (Choose at-least one course from the list) 801 Business Analytics 802 Industrial Safety 803 Operations Research 804 Cost Management of Engineering Projects 805 Composite Materials 806 Waste to Energy 807 Cyber Security	3	0	0	3
6	Project (PRJ-EV-525)	Mini Project and Seminar	0	0	4	2
7	Audit I (AUD-9XX)	Audit Course I	2	0	0	-
					Total	21

Semester III

Sr. No	Course Type / code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Dissertation (DIS-EV-601)	Dissertation Phase - I	0	0	28	14
					Total	14

Semester IV

Sr. No	Course Type / code	Course Name	Teaching Scheme			Credits
			L	T	P	
1	Dissertation (DIS-EV-602)	Dissertation Phase - II	0	0	28	14
					Total	14

Total Credits = 70

Audit course I

AUD-901 Project Management

AUD-902 Disaster Management

AUD-903 Sanskrit for Technical Knowledge

AUD-904 Value Education

AUD-905 Constitution of India

AUD-906 Pedagogy Studies

AUD-907 Stress Management by Ancient Indian Techniques

AUD-908 Personality Development through Life Enlightenment Skills

Open Elective

OEC-801 Business Analytics

OEC-802 Industrial Safety

OEC-803 Operations Research

OEC-804 Cost Management of Engineering Projects

OEC-805 Composite Materials

OEC-806 Waste to Energy

OEC-807 Cyber Security

Semester – I

M.Tech (ESD&VLSI) Course Syllabi (2018-2019)

PCC-EV-501 Semiconductor Devices (3-0-0-3)

Course Objectives:

1. Discuss the basic principles of quantum mechanics that apply to semiconductor material and device physics.
2. Derive the small signal equivalent circuit of the MOSFET and analyze the frequency limitations of the device.
3. Discuss non-ideal effects in MOSFETs.
4. Develop the fundamentals of nano-transistors.

Course Syllabus:

Unit 1: Semiconductor materials, crystal lattices, growth of semiconductors.

Unit 2: Energy bands and charge carriers in semiconductors, carrier concentrations, drift of carriers in electric and magnetic fields, excess carriers in semiconductors, diffusion of carriers.

Unit 3: Junctions, fabrication of p-n junctions, equilibrium conditions, forward and reverse biased junctions, reverse breakdown, transient and ac conditions, metal semiconductor junction.

Unit4:The MOSFET fundamentals, the two, three and four terminal MOSFE, MOS electrostatics, threshold voltage, CV characteristic, The basic MOSFET operation, substrate bias effects, small signal equivalent circuit and frequency limitation factors, deep submicron MOSFET concepts.

Unit 5: Small signal amplifiers using MOSFET and other semiconductor devices, The Ballistic MOSFET, the transmission theory of the MOSFET.

Course Outcomes:

At the end of this course, students will be able to

1. Appraise a semiconductor in thermal equilibrium.
2. To familiarize with the device fabrication technology.
3. Using the MOSFET to build basic digital and analog circuits.
4. Comparing non-ideal effects in different semiconductor devices.
5. Evaluate the performance of different MOSFETs.

References:

1. Solid state electronic devices, Ben G. Streetman, Sanjay Kumar Banerjee, 2006.
2. An introduction to semiconductor devices, Donald Neamen 2005.
3. Introduction to semiconductor materials and devices, M. S. Tyagi, 2008.
4. Semiconductor physics and devices, Donald Neamen, 2002.
5. The MOS transistor, YannisTsividis, Colin McAndrew, Oxford University Press, 2012.
6. The fundamentals of nanotransistors, Mark Lundstrom, World scientific, 2018.

PCC-EV-502 Real Time Embedded Systems (3-0-2-4)

Course Objectives:

1. Understand basics of embedded systems.
2. Study the architecture of ARM series microprocessor.
3. Understand need and application of ARM Microprocessors in embedded system.
4. Learn architecture and programming for ARM-7 and ARM Cortex-M3 Microcontroller.
5. Learn external interfacing of real world input and output devices with ARM.

Course Syllabus:

Unit 1: Embedded System Hardware: Embedded systems definition, characteristics, Common design Metrics, Processor technology, IC Technology, Design Technology, Hardware components like Microcontroller, GPP, ASSP, ASIP, SoC.

Unit 2: ARM Architecture: ARM Design Philosophy, Introduction to ARM processors and its versions, ARM7/ARM9/ ARM11 features, advantages & suitability in embedded application, ARM7 data flow model, programmer's model, modes of operations, Instruction set, programming in assembly language. ARM7 Based Microcontroller LPC2148: Features, Architecture (Block Diagram and Its Description), System Control Block (PLL and VPB divider), Memory Map, GPIO, Pin Connect Block, Interfacing with LED, LCD, GLCD, Key switch, KEYPAD, Relay, Stepper Motor.

Unit 3: Embedded Programming: Techniques of writing efficient C code for Microcontroller: C data types for ARM, Signed & unsigned data types, Storage class-Static and Extern, Volatile keyword, Operations on bits, Functions, ARM / Thumb procedural call standard, Pointers and Arrays, Conditional statements- if…else, Switch, Structure, Conditional loops- for and while, Preprocessing, Compiling, Cross compiling, Compiler driver, Startup code and board support packages, Program segments Calling assembly routines in HLL, Interrupt handling in C, Interrupt latency. Simple C Programs using Function Calls, Pointers, Structures, Integer and Floating-Point Arithmetic, Assembly Code using Instruction Scheduling, Register Allocation, Conditional Execution and Loops, MISRA standards for 'C' programming, CMSIS standards, DUX.gen standards.

Unit 4: Embedded Development Environment: Development Environment, Simulator, Emulator, Testing and debugging, Super Loop Approach, Validation and debugging of embedded systems, Hardware-software co-design in an embedded system, Real World Interfacing with ARM7 Based Microcontroller.

Unit 5: Interfacing to on chip LPC2148 peripherals: Timers, Counters, ADC/DAC using interrupt (VIC), UART, PWM, PLL, WDT, RTC, DMA, etc. Communication Protocols: Basic protocol concept, study of protocols like SPI, SCI, I2C, CAN, (EEPROM using I2C, SDCARD using SPI),

ARM Cortex M3 based interfacing for Ethernet, Wireless Protocols: IrDA, Bluetooth, IEEE802.11, Zig Bee, RF modules, GSM and GPS using UART.

Unit 6: Embedded System Applications: Digital Camera Example: Introduction, requirement Specification and design, Washing Machine, Automotive domain, Automatic Vending Machine, etc., Design Technology: Automation, Synthesis, verification, H/W and S/W co-simulation, IP cores, design process models.

Course Outcomes:

After successfully completing the course students will be able to:

1. Understand characteristics and technologies of embedded systems.
2. Describe the ARM microprocessor architectures and its feature.
3. Understand the functions and programming of various peripherals on ARM.
4. Understanding of ASM and C programming of ARM processor.
5. Design embedded system with available resources.

References:

1. Embedded Systems, (2nd ed.) by Raj Kamal (McGraw Hill), 2008.
2. Embedded Systems, Frank Vahid & Givargis, Wiley India, 2002.
3. Introduction to Embedded Systems by K.V. Shibu (McGraw Hill), 2009.
4. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M”, Newness, ELSEVIER.
5. ARM Systems Developer’s Guides- – A. N. Sloss, D. Symes, C. Wright, Elsevier 2008.
6. Embedded Microcomputer Systems, Real Time Interfacing – J.W. Valvano, Cole, 1999.
7. Embedded C - Michael J. Pont, 2nd Ed., Pearson Education, 2008.
8. LPC 214x User manual (UM10139):- www.nxp.com.
9. LPC 17xx User manual (UM10360):- www.nxp.com.

PCC-EV-503 Digital IC design (3-0-2-4)

Course Objectives:

1. To describe design metrics and fabrics.
2. To understand CMOS inverters, complex static and dynamic CMOS circuits.
3. To design various sequential circuits and building blocks and memories.
4. To explain floor planning and layout designs for different digital VLSI circuits.

Course Syllabus:

Unit 1: Metrics and Fabrics: Quality metrics of a digital design, the devices, diode, MOSFET, the manufacturing process, wires, electrical wire models, coping with interconnect, capacitive parasitic, resistive parasitic, inductive parasitic, advanced interconnect techniques.

Unit 2: Inverter: The CMOS inverter, evaluating the robustness of the CMOS inverter, static and dynamic behavior of CMOS inverter, power, energy and energy delay.

Unit 3: Complex CMOS Circuits: Designing combinational logic gates in CMOS, static CMOS design, dynamic CMOS design, perspectives.

Unit 4: Other Building Blocks: Designing sequential logic circuit, static latches and registers, dynamic latches and registers, alternative register styles, pipelining, sequential circuits, designing arithmetic building blocks, data paths in digital processor architectures, the multiplier, the shifter, other arithmetic operator, power and speed trade-offs in data path structures.

Unit 5: Memory: Designing memory and array structures, the memory core, memory peripheral circuitry, memory reliability and yield, power dissipation in memories, case studies in memory design.

Unit 6: Floor Planning and Layout Design: Transistor structures, wires and vias, scalable design rules, layouts of various gates, CMOS logic structures, clocking strategies, I/O structures, floor planning methods, off-chip connections, low power design strategies.

Course Outcomes:

At the end of this course, students will be able to:

1. Understand design flow, design metrics, devices, and interconnects with respect to various issues, parasitic effects, and implementation strategies for the design of digital integrated circuits.
2. Design CMOS inverters, complex static CMOS and complex dynamic CMOS circuits with various strategies to improve design metrics.
3. Design of arithmetic building blocks such as adders, multipliers, shifters, data path structures, and sequential digital logic for efficient implementation of the same for design metrics.

4. Design memories with efficient architectures to improve access times, power consumption.
5. Design examples of floor planning and layouts of digital VLSI circuits.

Reference and Text Books:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital integrated circuits, PHI, 2003.
2. Neil H. E. Weste, CMOS VLSI design, Pearson India, 2012.
3. M. Michael Vai, VLSI design (VLSI circuits), Taylor and Francis, 2000.
4. Douglas A. Pucknell and Kamran Eshraghian, Basic VLSI design, PHI, 1995.

PEC-EV-504 Modern Digital Design using Verilog (3-0-2-4)

Course Objectives:

1. To develop an understanding of designing a digital logic circuit/Arithmetic circuits/ Data paths based system to achieve a prescribed task on a generic platform.
2. To design a digital system, component (Processor), or process to meet a set of specifications using generic/Specific simulation and synthesis tools.
3. To understand and write codes for modeling of digital circuits both combinational (arithmetic) and sequential (FSM/ASM) using Verilog and simulate/synthesis the same using generic platform.
4. To recognize the need to use modern tools to assist problem solving.

Course Syllabus:

Unit 1: Review of logic design fundamentals: Combinational logic, logic simplification, Hazards in combinational networks.

Unit 2: Computer Arithmetic: Design of fixed point, floating point arithmetic units, MAC and SOP, CORDIC architectures, different types of adders, subtractors, multipliers and dividers.

Unit 3: Sequential machines: Concept of memory, design of clocked flip flops, practical clocking aspects concerning flip flops, clock skew, traditional approaches in sequential machine analysis and design, Reduction of state tables and state assignments.

Unit 4: Asynchronous FSM: Designing, cycles and races, hazards-static, dynamic and essential Hazards.

Unit 5: Design using Verilog: modules, Data flow, behavioral and structural types, design description, libraries, synthesis basics, mapping statements to Gates, model optimization, verification, test benches, Architectural synthesis, optimization, data path synthesis, logic level synthesis, examples of FSM, ASM, design of functions such as reciprocal, square root, sine, cosine, exponential, etc. Hardware testing and design for testability (DFT).

Unit 6: FPGA: Fundamental concepts, technologies, origin, Study of FPGA architectures, Configuration methods.

Course Outcome:

1. Ability to design arithmetic (fixed and floating point) circuits such as adders, Multipliers, Division Unit, square root, reciprocal, Sine-Cosine, Exponential etc.
2. Ability to design a simple processor with few arithmetic operations.
3. Understand the basic concepts of Verilog HDL

4. Write, simulate, create test bench for digital systems models in Verilog HDL

References:

1. William I Fleatcher, An Engineering approach to digital design, PHI.
2. Giovanni De Micheli, Synthesis andoptimization of digital circuit (McGraw Hill).
3. Charles H Roth, Jr., Fundamentals of Logic Design, Jaico Book.
4. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”,*PHI, 1999.*
5. J Bhaskar*, “A Verilog HDL Primer (3/e)”,* Kluwer, 2005.
6. Clive Max Maxfield, The Design Worriors Guide to FPGA Devices, tools and flows, Elsevier.
7. J.P. Hayes, Computer Architecture and Organization, McGraw Hill.
8. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson,2003.

PEC-EV-505 Digital Signal and Image Processing (3-0-2-4)

Course Objectives:

1. Develop a theoretical foundation of fundamental Digital Signal and Image Processing concepts.
2. Provide mathematical foundations for digital manipulation of images; image acquisition; preprocessing; segmentation; Fourier domain processing; and compression.
3. To develop Simulink model for Image and Signal processing applications using Simulink library in MATLAB.
4. To study VLSI architecture for implementation of image processing.

Course Syllabus:

Unit 1: Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

Unit 2: Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation.

Unit 3: Fixed point implementation of filters – challenges and techniques.

Unit 4: Digital Image Acquisition, Enhancement, segmentation, Digital Image Coding and Compression – JPEG and JPEG 2000.

Unit 5: Color Image processing – Handling multiple planes, computational challenges.

Unit 6: VLSI architectures for implementation of Image Processing algorithms, Pipelining.

Course Outcomes:

At the end of this course, students will be able to

1. Analyze discrete-time signals and systems in various domains.
2. Design and implement filters using fixed point arithmetic targeted for embedded platforms.
3. Evaluate the techniques for image enhancement and image restoration ,segmentation and compression
4. Compare algorithmic and computational complexities in processing and coding digital images.

References:

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition.
2. Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition.
3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006.

4. KeshabParhi, “VLSI Digital Signal Processing Systems – Design and Implementation”, Wiley India.
5. A. K. Jain, “Fundamentals of Digital Image Processing”, Prentice Hall.

PEC-EV-506 Object Oriented Programming (3-0-2-4)

Course Objectives:

1. To Gain knowledge about basic Programming language syntax and semantics to write programs and use concepts such as variables, conditional and iterative execution methods etc.
2. Understand the fundamentals of object-oriented programming paradigms defining classes, objects, invoking methods and exception handling mechanisms.
3. To identify the principles of inheritance, packages and interfaces.
4. To understand various OOPs concepts with the help of programs

Course Syllabus:

Unit 1: Object Oriented Programming Structured Programming and Object Oriented Programming paradigms.

Unit 2: Key Concepts: Data Abstraction: Class, object, constructors, and destructors, memory allocations for objects, member functions, and friend functions, templates. Inheritance: Single & multiple inheritances, virtual base class.

Unit 3: Polymorphism: Compile time polymorphism: operator overloading, function overloading, static binding. Run-time polymorphism: Virtual function, pure virtual function, abstract class, dynamic binding, Exception handling.

Unit 4: Object Oriented Design Object Oriented Design Approaches: Object Model, Dynamic Model, and Functional Model (Objet Diagram, State Diagram, and DFD).

Unit 5: Phases of Object Oriented Development: Object Analysis, System Design, Object Design.

Course Outcomes:

1. Describe the procedural and object oriented paradigm with concepts of streams, classes, functions, data and objects
2. Understand dynamic memory management techniques using pointers, constructors, destructors, etc
3. Describe the concept of function overloading, operator overloading, virtual functions and polymorphism.
4. Classify inheritance with the understanding of early and late binding, usage of exception handling, generic programming.
5. Demonstrate the use of various OOPs concepts with the help of programs

References:

1. Herbert Schild: The Complete Reference to C++, Osborne McGrawHill.
2. Bjarne Stroustrup: The C++ Programming Language, Addison Wesley.

3. Rambaugh et al.: Object Oriented Modeling and Design, PHI(EEE).
4. Grady Booch: Object Oriented Analysis and Design, Pearson Education.

PEC-EV-507 Computer Architecture (3-0-2-4)

Course Objectives:

1. To provide broad and deep knowledge of computer architecture issues and techniques.
2. Advanced hardware-based techniques for exploiting instruction level parallelism.
3. Knowledge of various architecture and techniques used for building High performance scalable Multithreaded and Multiprocessor system.
4. Understand Memory Hierarchy and Storage System.

Course Syllabus:

Unit 1: Fundamentals of Computer Design: Pipelining Basics, Major Hurdles of Pipelining, Overview of Instruction Set: Architecture and Operations, Different classes of Computers, Definition: Computer Architecture, Trends in Technology, Power of IC and Cost.

Unit 2: Instruction Level Parallelism (ILP): Introduction and Challenges, Basic Compiler Techniques for ILP, Dynamic Scheduling: Data Hazards, Algorithm and Examples, Statistic Scheduling, Exploiting ILP using Dynamic, Statistic Scheduling and Multiple Issue.

Unit 3: Limitation on ILP: Introduction, Limitations on ILP for Realization Processor, Crosscutting Issues: Hardware and Software Speculations, Multithreading: Thread-Level Parallelism.

Unit 4: Multiprocessor and Thread-Level Parallelism: Introduction, Symmetric Shared-Memory Architecture, Distributed Shared Memory and Directory-Based Coherence, Basics of Synchronization and Models for Memory Consistency.

Unit 5: Memory Hierarchy Design: Introduction, Optimization in Cache Performance, SRAM and DRAM, Virtual Memory and Machines, Crosscutting issues in Design of Memory Hierarchies.

Unit 6: Storage System: Introduction, Advanced Topics in Disk Storage, Real Faults and Failures: Definition and Examples.

Course Outcomes:

After successfully completion of Course Students will

1. Have broad understanding of the design of computer systems, including modern architectures and alternatives.
2. Be able to understand Instruction Level Parallelism at Hardware level.
3. Have knowledge of Multiprocessor and Thread-Level Parallelism.
4. Be able to visualize the Memory structure and Storage system.

References:

1. Kai Hwang, “Advanced Computer Architecture”, McGraw Hill Education, 1993.
2. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing” McGrawHill Education, 2012.
3. William Stallings, “Computer Organization and Architecture, Designing for Performance”, Prentice Hall, 6th edition, 2006.
4. Kai Hwang, “Scalable Parallel Computing”, McGraw Hill Education, 1998.
5. Harold S. Stone “High-Performance Computer Architecture”, Addison-Wesley, 1993.

PEC-EV-508 High Speed Digital Design (3-0-2-4)

Course Objectives:

1. Compare the performance High and low speed ADCs.
2. To develop insight into the design issues of high speed digital circuits.
3. To appraise noise sources and parasitic in high speed digital circuits.
4. To familiarize and create CAD tools for high speed digital circuits.

Course Syllabus:

Unit 1: High Speed ADCs Fundamental of high speed sampling, Base band antialiasing filters, Study of Harmonic sampling and bandpass sampling, Direct IF to digital conversion.

Unit 2: Distortion and noise in an ideal N bit ADC, AD9220 12-bit ADC, Spurious free Dynamic Range, Measurement of Noise Power Ratio, Flash converters, Case study of AD9066, Study of latency of ADCs.

Unit 3: High Speed ADC Applications Driving ADC inputs for low distortion and wide dynamic range, Applications of high speed ADCs in CCD imaging, high speed ADC applications in Digital transceivers.

Unit 4: High Speed DACs and DDS Systems Introduction to DDS, Aliasing in DDS Systems, 125 MSPS DDS System case study AD9850, DDS systems as ADC Clock Drivers, Amplitude modulation in a DDS System.

Unit 5: The AD9831 Complete DDS System, High Speed low distortion DAC architecture, High Speed interpolating DACs, QPSK signal generation using DDS.

Unit 6: Design issues of high speed Electronics Simulation tools, Prototyping Circuits, Grounding in high speed systems, Power supply noise reduction and filtering, Power supply conditioning, EMI/RFI considerations, Shielding concepts.

Course Outcomes:

1. Students shall become familiar with and application of many high speed signal processing building blocks such as amplifiers, ADCs, DACs, etc.
2. System applications are of broad general interest or emerging market trends.
3. The proper application of high speed devices also requires a thorough knowledge of good hardware design techniques, such as simulation, prototyping, layout, decoupling, and grounding. In the last section students become familiar with these issues as well as EMI and RFI design considerations.

References:

1. High-Speed Digital Design: A Handbook of Black Magic by Howard Johnson
2. High Speed Signal Propagation: Advanced Black Magic by Howard W. Johnson
3. Signal Integrity Issues and Printed Circuit Board Design by Douglas Brooks
4. High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by Stephen H. Hall
5. Signal Integrity - Simplified by Eric Bogatin.
6. Handbook of Digital Techniques for High-Speed Design: Design Examples, Signaling and Memory Technologies, Fiber Optics, Modeling, and Simulation to Ensure ... (Prentice Hall Modern Semiconductor Design) by Tom Granberg.
7. Noise Reduction Techniques in Electronic Systems, 2nd Edition by Henry Ott.
8. High Speed Design Techniques, Manual by analog Devices, October 1996.

PEC-EV-509 CAD of Digital System (3-0-2-4)

Course Objectives:

1. To prepare the student to understand the VHDL language feature to realize the complex digital systems.
2. To design and simulate sequential and concurrent techniques in VHDL
3. To explain modeling of digital systems using VHDL and design methodology
4. To Understand behavioral, non-synthesizable VHDL and its role in modern design
5. Students must be able to implement logic on an FPGA and a CPLD.

Course Syllabus:

Unit 1: An overview of design procedures for system design using CAD tools. Design verification tools. Examples using commercial PC based VLSI CAD tools. Design methodology based on VHDL, Basic concepts and structural descriptions in VHDL.

Unit 2: Characterizing hardware languages, objects and classes, signal assignments, concurrent and sequential assignments, Structural specification of hardware.

Unit 3: Design organization, parameterization and high level utilities, definition and usage of Subprograms, packaging parts and utilities, design parameterization, design configuration, design libraries, Utilities for high-level descriptions.

Unit 4: Data flow and behavioral description in VHDL- multiplexing and data selection, state Machine description, open collector gates, three state bussing, general dataflow circuit, updating basic utilities, Behavioral description of hardware.

Unit 5: CPU modeling for discrete design- Parwan CPU, behavioral description, bussing structure,data flow, test bench, a more realistic Parwan. Interface design and modeling. VHDL as a modeling language. MCMS-VHDL implementation of simple circuits using VHDL.

Course Outcomes:

At the end of the course student will be able

1. Model, simulate, verify, and synthesize with hardware description languages.
2. Design digital logic circuits in different types of modeling
3. Use computer-aided design tools for design of complex digital logic circuits.
4. Understand and use major syntactic elements of VHDL - entities, architectures, processes, functions, common concurrent statements, and common sequential statements

References:

1. *Z.Navabi, "VHDL Analysis and Modeling of Digital Systems", (2/e), McGraw Hill, 1998.*
2. *Perry, "VHDL (3/e)", McGraw Hill.2002*
3. A. Dewey, "Analysis and Design of Digital Systems with VHDL", CL-Engineering,1996.
4. Z.Navabi,"VHDL: modular design and synthesis of cores and systems", McGraw,2007.
5. C. H. Roth, Jr., L.K.John, "Digital Systems Design Using VHDL - Thomson LearningEMEA", Limited, 2008.
6. Recent literature in Analysis and Design of Digital Systems using VHDL.

PEC-EV-510 IC Technology (3-0-2-4)

Course Objectives:

1. To teach fundamental principles of fabrication of VLSI devices and circuits.
2. To provide knowledge about novel VLSI devices.

Course Syllabus:

Unit 1: Crystal growth, wafer fabrication, and basic properties of Silicon wafers, crystal structure and growth methods, crystal defects, Wafer cleaning, clean room concepts.

Unit 2: Lithography, optical, deep UV techniques, photo resist, exposure and development, E-beam lithography, X-ray lithography.

Unit 3: Thermal oxidation and Si-SiO_2 interface, manufacturing methods – dry and wet oxidation, thin and thick film oxide growth kinetics, models of oxidation kinetics, polysilicon oxidation, silicide oxidation, Si-SiO_2 interface charge.

Unit 4: Dopant diffusion, measurement methods, models and simulation, ion implantation, models and simulation, Thin film deposition- manufacturing methods, measurement methods, models and simulation.

Unit 5: Etching- manufacturing methods, measurement methods, models and simulation, Wet chemical etching, dry physical etching, dry chemical etching, reactive ion etching, ion beam techniques Device Isolation, Contacts and Metallization, CMOS Design flow N-well , P-well, Twin tub process, Measurements, Packaging and Testing of IC.

Unit 6: Novel devices: Nanowire -Fabrication , application ; Graphene device- Carbon nanotubes fabrication ,CNT application

Course Outcomes:

1. Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.
2. Demonstrate a clear understanding of various MOS fabrication processes, semiconductor measurements, packaging, testing and advanced semiconductor technologies.
3. Discuss physical mechanism in novel devices.
4. Verify processes and device characteristics via simulations.

References:

1. James D. Plummer, Michael D. Deal, Peter B. Griffin, SILICON VLSI technology, Pearson India, 2011.
2. Dieter K. Schroder, Semiconductor material and device characterization, Wiley-Blackwell; 2006.
3. Sorab K. Gandhi, “VLSI Fabrication Principles”, Wiley, Student Edition.

4. 4. G. S. May and S. M. Sze, “Fundamentals of Semiconductor Fabrication”, Wiley, First Edition.
5. James E. Morris and Krzysztol Iniewski, “Nanoelectronic Device Applications Handbook”, CRC Press
6. Stephen A. Campbell, “The Science and Engineering of Microelectronic Fabrication”, Oxford University Press, 2nd Edition.

PEC-EV-511 Parallel Processing (3-0-2-4)

Course Objectives:

1. To provide knowledge about Parallel Processing and Pipelining.
2. To analyze Parallel Software Issues and to study advanced pipelining techniques and VLIW processors.
3. To identify issues and solutions for multithreaded processors.
4. To study operating systems for multiprocessor systems

Course Syllabus:

Unit 1: Overview of Parallel Processing and Pipelining, Performance analysis, Scalability.

Unit 2: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

Unit 3: VLIW processors; Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

Unit 4: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions.

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues.

Unit 6: Operating systems for multiprocessors systems customizing applications on parallel processing platforms.

Course Outcomes:

At the end of this course, students will be able to

1. Identify limitations of different architectures of computer
2. Analysis quantitatively the performance parameters for different architectures
3. To identify issues and solutions for multithreaded processors.
4. Investigate issues related to compilers and instruction set based on type of architectures.

References:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition.
2. Kai Hwang, “Advanced Computer Architecture”, TMH.
3. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.

4. William Stallings, “Computer Organization and Architecture, Designing for performance” Prentice Hall, Sixth edition.
5. Kai Hwang, ZhiweiXu, “Scalable Parallel Computing”, MGH.
6. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan Kaufmann.

PEC-EV-512 Programmable Digital Signal Processors (3-0-2-4)

Course Objectives:

1. The purpose of this course is to introduce the concepts of PDSP Processor and its architectures.
2. To program DSP Processor for various applications.

Course Syllabus:

Unit 1: Programmable Digital Signal Processors: Commercial Digital Signal-Processing Devices, Data Addressing Modes of TMS320C54XX DSPs, Data Addressing Modes of TMS320C54XX Processors, Memory Space of TMS320C54XX Processors, Program Control.

Unit 2: TMS320C54XX Instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

Unit 3: Implementations of Basic DSP Algorithms: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

Unit 4: Implementation of FFT Algorithms: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and Scaling, Bit-Reversed Index Generation, An 8-Point FFT Implementation on the TMS320C54XX, and Computation of the Signal Spectrum.VR10 Regulations.

Unit 5: Interfacing Memory and I/O Peripherals to Programmable DSP devices I: Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts And I/O, Direct Memory Access (DMA).

Unit 6: Interfacing Memory and I/O Peripherals to Programmable DSP Devices -II:A Multi-channel Buffered Serial Port (MCBSP), MCBSP Programming, A CODEC Interface Circuit, CODEC Programming, a CODEC-DSP Interface Example.

Course Outcomes:

1. Students are aware of the basic architectural features that programmable DSP devices should have, their operations & their computational accuracies in DSP implementation.
2. Students will be able to use the DSP processors TMS 320C 54XX for implementation of DSP algorithms & its interfacing techniques with various I/O peripherals.
3. Students will be able to use MATLAB DSP toolbox for analysis & design of DSP.

References:

1. DSP Processors and Architectures, Avatar Singh and S.Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Feature, Lapsley et al, S. Chand & Co. 2000.
3. Digital Signal Processors, Architecture, Programming and Applications, B. Venkataramani and M. Bhaskar, TMH, 2002.

4. Digital Signal Processing, Jonatham Stein, John Wiley, 2005.

MCC-590 Research Methodology and IPR (2-0-0-2)

Course Objectives:

1. To explain formulation and analysis of research problem.
2. To describe research ethics and technical writing.
3. To understand IPR and patent rights.
4. To demonstrate new developments in IPR with the help of case studies.

Course Syllabus:

Unit 1: Meaning of research problem, sources of research problem, criteria characteristics of a good research problem, errors in selecting a research problem, scope and objectives of research problem, Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, necessary instrumentations.

Unit 2: Effective literature studies approaches, analysis plagiarism, and research ethics.

Unit 3: Effective technical writing, how to write report, paper developing a research proposal, format of research proposal, a presentation and assessment by a review committee.

Unit 4: Nature of intellectual property: Patents, designs, trade and copyright, process of patenting and development: technological research, innovation, patenting, and development. International scenario: international cooperation on intellectual property, procedure for grants of patents, patenting under PCT.

Unit 5: Patent rights: Scope of patent rights, licensing and transfer of technology, patent information and databases, geographical indications.

Unit 6: New developments in IPR: administration of patent system, new developments in IPR; IPR of biological systems, computer software etc. traditional knowledge case studies, IPR and IITs.

Course Outcomes:

At the end of this course, students will be able to:

1. Understand research problem formulation.
2. Analyze research related information and follow research ethics.
3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
4. Understanding that when IPR would take such important place in growth of individuals and nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general and engineering in particular.

5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R and D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

References:

1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science and engineering students”.
2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”.
3. Ranjit Kumar, 2 ndEdition , “Research Methodology: A Step by Step Guide for beginners”.
4. Halbert, “Resisting Intellectual Property”, Taylor and Francis Ltd ,2007.
5. Mayall , “Industrial Design”, McGraw Hill, 1992.
6. Niebel , “Product Design”, McGraw Hill, 1974.
7. Asimov , “Introduction to Design”, Prentice Hall, 1962.
8. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.
9. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008.

MAC-591 English for Research Paper Writing (2-0-0-0)

Course objectives:

1. To understand that how to improve your writing skills and level of readability.
2. To learn about what to write in each section.
3. To understand the skills needed when writing a Title.
4. To ensure the good quality of paper at very first-time submission.

Course Syllabus:

Unit 1: Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.

Unit 2: Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, and introduction.

Unit 3: Review of the Literature, Methods, Results, Discussion, Conclusions, the Final Check.

Unit 4: Key skills are needed when writing a Title; key skills are needed when writing abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature.

Unit 5: Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, and skills are needed when writing the Conclusions.

Unit 6: Useful phrases, how to ensure paper is as good as it could possibly be the first- time submission.

Course Outcomes:

At the end of course, student will be able to:

1. Understand how to plan and prepare concise writings by using appropriate words and structured paragraphs.
2. Explain how to write different sections such as abstracts, introduction, survey, methodology, results, conclusions, etc. in paper and reports.
3. Describe key skills needed for writing title of a paper or report.

References:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books).
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press.
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book.
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Semester – II

PCC-EV-513 Analog and Mixed Signal VLSI Design (3-0-2-4)

Course Objectives:

1. To understand basics of analog devices.
2. To explain different configurations of single stage amplifiers and their frequency response.
3. To describe and analyze current mirrors.
4. To represent noise in various analog circuits and its effects and removal techniques.
5. To analyze and design OP-AMPs and other analog and mixed signal blocks and band gap references.

Course Syllabus:

Unit 1: Introduction and Devices: Introduction to analog IC design, diode, BJT and MOSFET as analog devices, device models including parasitic capacitances.

Unit 2: Current Mirrors: Passive and active current mirrors, basic current mirrors, cascode current mirrors, active current mirrors, large and small signal analysis, common mode properties.

Unit 3: Amplifiers: Common source, source follower, common gate, cascade, folded cascode, basic differential pair, common mode response, single ended differential operation, differential pair with MOS loads, frequency response of all amplifiers, association of poles with nodes.

Unit 4: Noise and Feedback: Representation of noise in circuits, noise in single stage amplifiers and cascade stages, noise in differential pairs, noise bandwidth, general feedback considerations, feedback topologies, effect of loading, effect of feedback on noise.

Unit 5: Operational amplifiers: One stage and two stage op amps, gain boosting, common mode feedback, input range limitation, slew rate, power supply rejection, noise in op-amp, stability and frequency compensation, multi pole system, phase margin, frequency compensation, compensation of two stage op-amps, other compensation techniques.

Unit 6: Other Analog and Mixed Signal Blocks: Band gap references, supply independent biasing, temperature independent references, PTAT current generation, speed and noise issues, introduction to other analog blocks such as S/H circuits, ADC, DAC, Sigma-Delta Converters, PLL/DLL, etc.

Course Outcomes:

At the end of this course, student will be able to analyze and design:

1. Basic building blocks like current/voltage sources and basic gain stages.
2. Advanced analog circuits such as cascaded stages, cascade, differential amplifiers.
3. OPAMPs, Band gap reference circuits

4. Mixed signal circuits such as S/H circuits, ADC, DAC, Sigma-Delta Converters, PLL/DLL.

References:

1. Behzad Razavi, Design of Analog CMOS integrated circuits, Tata McGraw Hill Edition, 2002
2. Philip E Allen, Douglas R. Holberg, CMOS Analog Circuit Design, Oxford, 2002
3. David A Johns, Ken Martin, Analog Integrated Circuit Design, Wiley Students edition, 2002

PCC-EV-514 Advanced Verification Techniques using System Verilog (3-0-2-4)

Course Objectives:

1. This course discusses fundamental Verilog concepts of today's most advanced digital design techniques. it offers broad coverage of Verilog HDL from a practical design perspective.
2. Introduces students to gate, dataflow (RTL), behavioral, and switch level modeling, describes leading logic synthesis methodologies; explains timing and delay simulation; and introduces many other essential techniques for creating tomorrows complex digital designs.

Course Syllabus:

Unit 1: Verification: Advanced Test Bench Structures, Evolution of verification techniques. Role of re-use in verification. Verification stages in ASIC design flow, understanding sign off criteria for verification. Transaction level modeling (TLM): Fundamentals of TLM.

Unit 2: System Verilog Basics of SV: User defined types, Enumeration, Casting, Parameterized types Dynamic Arrays, Associative Arrays, Queues/Lists, Structures System Verilog Scheduler, Program Control, structures, Packages, Tasks & Functions, Dynamic Processes Control Interposes Sync & Communication, Semaphore, mailbox.

Unit 3: Classes: Constructors, Inheritance, Virtual methods, Protection, Parameterized classes, Polymorphism, Virtual Classes Interfaces: Interface, Virtual Interfaces. Randomization& Constraints: Stimulus Generation techniques, Constraint blocks, Randomize, Random sequences.

Unit 4: Functional Coverage: Cover group, Cover point, Cross Coverage methods.SV-Assertions: Immediate assertions, Concurrent assertions, Boolean Expressions, Sequences, Property Block, Verification Directives, Local Data values.DPI: Matlab-SV integration, C models to SV integration.

Unit 5: UVM: UVM Transactions, Core Utility Functions and Implementation UVM Components, Phases, Creating Components & Running the Simulation, Factory, Starting the Test, Ending the Test, Connection to the DUT Transactions, Configuration, UVM Resources and config_db. Introduction to Sequences: Sequence Elements, Sequences, Sequencers, Drivers to Sequencer to sequence Connection, Virtual Sequences, Prioritized Item Selection and Arbitration.

Unit 6: UVM Registers: The Register Model, Creating Register Models, Integrating Register Models, Backdoor Access. Project and lab work: Pick up any open core design and develop verification environment around it using SV-UVM, Maximum group of 3 students in one project and we can insist re-use of code among different groups. Maximum weighted will be given to the code which is re-usable across projects. For system Verilog IEEE 1800-2012 document should be reference book to all the students. Exam should be conducted on examples given in LRM document.

Course Outcomes:

1. Able to apply the Simulation and Synthesis of Digital Circuits.
2. Explain the design of Test benches.
3. Able to explain the System Modeling with Tasks and Functions.
4. Design of digital circuits using different modeling styles.

References:

1. System Verilog Assertions by Srikanth Vijayaraghavan, Meyyappan Ramanathan Publisher: Springer.
2. IEEE 1800-2012 SV LRM.
3. Getting Started with UVM: A Beginner's Guide Kindle Editionby Vanessa R. Cooper.
4. Doulos UVM Golden Reference Guide Kindle Editionby John Aynsley, David Long, Doug Smith.
5. System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modelling Hardcover by P. Moorby, Stuart Sutherland, Simon Davidmann.
6. System Verilog for Verification: A Guide to Learning the Test Bench Language Featuresby Chris Spear, Greg Tumbush.
7. IEEE 1666-2011.https://verificationacademy.com/

PEC-EV-515 Low Power VLSI Design (3-0-2-4)

Course Objectives:

1. Developing insight into digital COMS IC power dissipation issues.
2. To illustrate circuit techniques for low power design.
3. To compare low power memory design issues.
4. Applying low power techniques for VLSI system design and applications.

Course Syllabus:

Unit 1: Low power Basics: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Unit 2: Device & Technology Impact on Low Power: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit 3: Power estimation Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems.

Unit 4: Low Power Design Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Unit 5: Low power Architecture & Systems: Power & performance management, switching activity Reduction, parallel architecture with voltage reduction, flow graph transformation, low power Arithmetic components, low power memory design.

Unit 6: Low power Clock Distribution: Power dissipation in clock distribution, single driver vs distributed buffers, Zero skew vs. tolerable skew, chip & package co-design of clock networkAlgorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Course outcomes:

1. Identify the sources of power consumption in a given VLSI Circuit.
2. Analyze and estimate dynamic, leakage power components in a DSM VLSI circuit.
3. Choose SRAMs/ DRAMs for Low power applications.
4. Design low power arithmetic circuits and systems.
5. Decide at which level of abstraction it is advantageous to implement low power techniques in a VLSI system design.

References:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997.
3. Kaushik Roy, SharatPrasad,“Low-Power CMOS VLSI Circuit Design” Wiley,2000.
4. Kiat-Seng Yeo, Kaushik Roy, Low-voltage, low-power VLSI subsytems, McGraw Hill 2017.

PEC-EV-516 Memory Technologies (3-0-2-4)

Course Objectives:

1. Understand the basic device physics of semiconductor memory devices.
2. Demonstrate a familiarity with major memory device structures and integration technology and apply device models to analyze various types of memory devices.
3. Establish a good knowledge base about the emerging advance memory technologies.

Course Syllabus:

Unit 1: Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

Unit 2: DRAMs, MOS DRAM Cell, Bi-CMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

Unit 3: Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Unit 4: Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Unit 5: Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Unit 6: Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging.

Course outcomes:

At the end of the course, students will be able to:

1. Select architecture and design semiconductor memory circuits and subsystems.
2. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
3. Knowhow of the state-of-the-art memory chip design.

References:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience.

2. KiyooItoh, “VLSI memory chip design”, Springer International Edition.
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability, PHI.

PEC-EV-517 Physical Design Automation (3-0-2-4)

Course Objectives:

1. Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2. Discuss the concepts of design optimization algorithms and their application to physical design automation.
3. Understand the concepts of simulation and synthesis in VLSI Design Automation.
4. Formulate CAD design problems using algorithmic methods.

Course Syllabus:

Unit 1: Introduction to VLSI Physical Design Automation.

Unit 2: Standard cell, Performance issues in circuit layout, delay models Layout styles.

Unit 3: Discrete methods in global placement.

Unit 4: Timing-driven placement. Global Routing Via Minimization.

Unit 5: Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing.

Unit 6: Compaction, algorithms, Physical Design Automation of FPGAs.

Course Outcome (CO):

At the end of the course, students will be able to:

1. Study automation process for VLSI System design.
2. Understanding of fundamentals for various physical design CAD tools.
3. Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

References:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, JohnWiley, 1998.
2. N.A.Sherwani , “Algorithms for VLSI Physical Design Automation”, (3/e), Kluwer,1999.
3. S.M. Sait , H. Youssef, “VLSI Physical Design Automation”, World scientific, 1999.
4. M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996.

PEC-EV-518 Testability of VLSI Circuits (3-0-2-4)

Course Objectives:

1. Understand the concepts of VLSI circuits testing.
2. To provide knowledge of various modeling use for VLSI testing.

Course Syllabus:

Unit 1: Fault Modeling and Test Generation: Importance of Testing. Testing during the VLSI Lifecycle. Challenges in the VLSI Testing: Test Generation, Fault Models. Levels of abstraction in VLSI Testing, Historical Review of VLSI Test Technology, Functional Versus Structural Testing. Levels of Fault Models, Single Stuck-at Fault. Testability measures: Controllability and Observability.

Unit 2: Fault Simulation: Serial, Parallel, deductive, Concurrent, Fault Sampling. Combinational Test Generations: Random Test generation, ATPG for Combinational Circuits: D-Algorithm, PODEM. Sequential Circuit Test Generations: ATPG for single-clock synchronous circuits, Designing a Sequential ATPG, Untestable Fault Identification.

Unit 3: Design for Testability: Design for Testability Basics: AdHoc Approach, Structured Approach. Scan Cell Designs. Scan Architectures. Scan Design Rules. Scan Design Flow. Special-Purpose Scan Designs. RTL Designfor Testability.

Unit 4: Logic Built-In Self-Test: BIST Design Rules: Unknown Source Blocking, Re-Timing. Test Pattern Generation: Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing. Output Response Analysis. Logic BIST Architectures: BIST Architectures for Circuits with and without Scan Chains, BIST Architectures Using Register Reconfiguration. Fault Coverage Enhancement: Test Point Insertion, Mixed-Mode BIST, Hybrid BIST.

Unit 5: Test Compression and Boundary Testing: Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes. Test Response Compaction: Space Compaction, Time Compaction, Mixed Time and Space Compaction, Digital Boundary Scan (IEEE Std. 1149.1).

Unit 6: Analog and Mixed-Signal Testing: Analog and Mixed-Signal Circuit Trends. Functional DSP-Based Testing. Static ADC and DAC Testing Methods. Analog Fault Models. Types of Analog Testing. Analog Fault Simulation. Introduction to IDDQ Test.

Course Outcome (CO):

1. Recognize Faults and classify different fault detection in VLSI Systems design at various levels.
2. Designs develop algorithms for analysis of faults and test methodology.
3. Understand analog and mixed signal testing

References:

1. Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, “Vlsi Test Principles And Architectures” The Morgan Kaufmann, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, “Essentials Of Electronic Testing For Digital, Memory And Mixed-Signal Vlsi Circuits”, Kap, 2002.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
4. Alexander Miczo, “Digital Logic Testing and Simulation” 2/E, A John Wiley & Sons, 2003.
5. Charles E. Stroud, “A Designer's Guide to Built-In Self-Test”, Kap. 2002.
6. Z. Navabi, “Digital System Test and Testable Design”, Springer, 2011.

PEC-EV-519 VLSI Signal Processing (3-0-2-4)

Course Objectives:

1. Design and optimize VLSI architectures for basic DSP algorithms.
2. Optimizing digital filters for performance.
3. Design and analyze low power DSP architectures for high performance.
4. Develop some signal processing applications using FPGA.

Course Syllabus:

Unit 1: Introduction, Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation.

Unit 2: Methods of critical path reduction, Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) –Pipelining and parallel processing – retiming – unfolding – systolic architecture design.

Unit 3: Algorithmic strength reduction methods and recursive.

Unit 4: Filter Design Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters, design.

Unit 5: Design of pipelined digital filters -Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

Unit 6: Synchronous asynchronous pipelining and programmable DSP- Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

Course outcomes:

1. Comprehension of VLSI design methodology for signal processing systems.
2. Compare different VLSI algorithms for using in a particular application.
3. Develop DSP algorithms using pipelining and parallel processing approaches.
4. Implement basic architectures for DSP using CAD tools.

References:

1. KeshabK.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, Indian Reprint, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.

3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995.

PEC-EV-520 SOC Design (3-0-2-4)

Course Objectives:

1. To familiar with ASIC design flow.
2. To identify software and testability challenges in SoC.
3. Specifically, the class project involves FPGA prototyping platform using state-of- the-art synthesis and verification tools and design flows.

Course Syllabus:

Unit 1: ASIC - Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.

Unit 2: NISC - NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

Unit 3: Simulation - Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Unit 4: Low power SoC design / Digital system, - Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

Unit 5: Synthesis - Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.

Unit 6: Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

Course outcomes:

At the end of the course, students will be able to:

1. Identify and formulate a given problem in the framework of SoC based design approaches.
2. Design SoC based system for engineering applications.
3. Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development.

References:

1. Hubert Kaeslin, “Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication”, Cambridge University Press, 2008.
2. B. Al Hashimi, “System on chip-Next generation electronics”, The IET, 2006.
3. RochitRajsuman, “System-on- a-chip: Design and test”, Advantest America R & D Center, 2000.
4. P Mishra and N Dutt, “Processor Description Languages”, Morgan Kaufmann, 2008.
5. Michael J. Flynn and Wayne Luk, “Computer System Design: System-on-Chip”. Wiley, 2011.

PEC-EV-521 Embedded Networking (3-0-2-4)

Course Objectives:

1. To Understand the Architectural Overview of IoT.
2. To Understand the IoT Reference Architecture and Real-world Design Constraints.
3. To understand the various IoT Protocols (Data link, Network, Transport, Session, Service).

Course Syllabus:

Unit 1: Overview: Iot-An Architectural Overview– Building An Architecture, Main Design Principles And Needed Capabilities, An Iot Architecture Outline, Standards Considerations.

Unit 2: M2M and Iot Technology Fundamentals- Devices and Gateways, Local and Wide Area Networking, Data Management, Business Processes inIot, Everything as A Service (Xaas), M2M and Iot Analytics, Knowledge Management.

Unit 3: Reference Architecture: Iot Architecture-State Of The Art – Introduction, State Of The Art, Reference Model And Architecture, Iot Reference Model - Iot Reference Architecture- Introduction, Functional View, Information View, Deployment And Operational View, Other Relevant Architectural Views. Real-World Design Constraints- Introduction, Technical Design Constraints-Hardware Is Popular Again, Data Representation And Visualization, Interaction And Remote Control.

Unit 4: IoT Data Link Layer &Network Layer Protocols: PHY/MAC Layer(3GPP MTC, IEEE 802.11,IEEE 802.15),Wireless HART, Z-Wave, Bluetooth Low Energy, Zigbee Smart Energy, DASH7 - Network Layer-Ipv4, Ipv6, 6lowpan, 6tisch,ND, DHCP, ICMP, RPL, CORPL, CARP.

Unit 5: Transport & Session Layer Protocols: Transport Layer (TCP, MPTCP, UDP, DCCP, SCTP)-(TLS, DTLS) – Session Layer-HTTP, Coap, XMPP, AMQP, MQTT.

Unit 6: Service Layer Protocols & Security: Service Layer -Onem2m, ETSI M2M, OMA, BBF – Security In Iot Protocols – MAC 802.15.4, 6lowpan, RPL, Application Layer.

Course Outcomes:

After successfully completing the course students will be able to:

1. To Understand the Architectural Overview of IoT.
2. Describe the difference between Wired and Wireless protocols.
3. Understand the IoT Reference Architecture and Real-world Design Constraints.
4. Understand different communication protocols e.g. Zigbee, bluetooth Ethernet protocol
5. To understand the various IoT Protocols (Datalink, Network, Transport, Session, Service).

References:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Edition, Academic Press, 2014.
2. Peter Waher, “Learning Internet of Things”, PACKT publishing, BIRMINGHAM – MUMBAI.
3. Bernd Scholz-Reiter, Florian Michahelles, “Architecting the Internet of Things”, ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer.
4. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6: The Evolving World of M2M Communications”, ISBN: 978-1-11847347-4, Willy Publications.
5. Vijay Madisetti and ArshdeepBahga, “Internet of Things (A Hands-onApproach)”, 1st Edition, VPT, 2014.
6. http://www.cse.wustl.edu/~jain/cse570-15/ftp/iot_prot/index.html.

PEC-EV-522 System Design with Embedded Operating System (3-0-2-4)

Course Objectives:

1. To make the students aware of the need of real time systems.
2. To understand basic issues for real time OS issues.
3. To study uCOS-II as a case study of RTOS.
4. To acquire skill of using uCOS.
5. To make students aware of the embedded linux operating system.

Course Syllabus:

Unit 1: Real Time Systems Concepts: Real Time Systems, Characteristics, Hard and Soft Real Time Systems, Critical section of code, Resource, Shared resource, multitasking, Task, Context switch, Kernel, Scheduler, Dispatcher, Preemptive Kernel, Non-Preemptive Kernel, Reentrancy, Round robin scheduling, Task Priorities, Static & Dynamic Priority, Priority Inversion, Assigning task priorities, Mutual Exclusion, Deadlock, Clock Tick, Memory requirements, Advantages & disadvantages of real time kernels.

Unit 2: µCOS II:History and Definition of RTOS, Key Characteristics of RTOS, Features of µCOS II, Kernel structure, µCOS II RTOS services: Task management: Tasks, Task states and Control block, Task scheduling, task level context, switching, Idle task, Time management: Clock Tick, Implementing delay in RTOS, resuming the delayed task, getting system time, Placing task in ECB wait list, Removing a task from ECB, List of Free ECBs, Initializing an ECB, Making a Task Ready and wait for and event. Implementing timeout in RTOS.

Unit 3: Inter-Task Communication and Synchronization: Semaphore, Creating/deleting a Semaphore, Waiting, signaling semaphore, Mutex, Creating/deleting and handling Mutex, Event flag management, Timer Interrupt Service Routines (ISR), Soft Timers, Mail box, sending / getting a message using mailbox as semaphore, message queue and its management, Memory control block. Case studies of uCOS based applications.

Unit 4: Embedded Linux Development Environment : Need of Linux, Embedded Linux Today, Open Source and the GPL, BIOS and Boot loader, Anatomy of an Embedded System, Storage Considerations, Embedded Linux Distributions, Processors for embedded Linux stand alone and integrated processors, ARM9 architecture and ARM9 based processors. ARM flavors and features of various chipsets/architectures, Anatomy of embedded Linux setup, Booting and Initialization of Kernel. Storage considerations, Flash file systems, Execution contexts, Commercial embedded Linux distributions, Embedded Development Environment, Cross-Development Environment, Development Tools, GNU Debugger, Tracing and Profiling Tools, Binary Utilities, Overview of Commands, File I/O (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

Unit 5: Linux Kernel Construction: Linux Kernel Background, Linux Kernel Construction, Kernel Build System, Kernel Configuration, Role of a Bootloader, Bootloader Challenges. A Universal Bootloader : Das Boot, Porting U-Boot, Device Driver Concepts, Module Utilities, Driver Methods, Linux File System & Concepts.

Unit 6: Embedded Software Development, Testing Process and Tools: Embedded Software development process and tools, Host and Target Machines, Target System Tools and Image transfer, Embedded Loader, Monitor, linking and Locating Software, Getting Embedded Software into the Target System, Issues in Hardware- Software Design and Co-design. Testing on Host Machine, Simulators, Laboratory Tools, Case study of embedded system like Automatic Chocolate Vending Machine, Mobile Phone.

Course Outcome:

1. Identify need of Real Time Systems.
2. Able to port uCOS-II operating system on ARM7/AMR Cortex M3 Board.
3. Able to compltere 5 programs in uCOS-II on ARM7/Cortex M3.
4. Understand ARM9 architecture and Linux as in embedded hardware.
5. To install Linux and use bootloader and Complete at least 5 assignments based of programming the embedded linux.

References:

1. MicroC OS II: The Real Time Kernel Jean J. Labrosse CMP books.
2. Real-Time Concepts for Embedded Systems Qing Li, Caroline Yao Elsevier.
3. Simple Real-time Operating System: A Kernel, ChowdaryVenkateswara, Amazon.
4. Christopher Hallinan, “Embedded Linux Primer -A Practical, Real-World Approach ”2nd ed., Prentice Hall.
5. Building Embedded Linux Systems, KarimYaghmour, Jon Masters, Gilad Ben-Yossef, Philippe Gerum, O'Reilly Media; Second Edition edition (August 22, 2008).
6. Embedded Linux System Design and Development b P Raghvan, Amol Lad, SriramNeelakandan, Auerbach Publications.
7. Advanced UNIX Programming, Richard Stevens.

PEC-EV-523 Communication Buses and Interfaces (3-0-2-4)

Course Objectives:

1. To identify different serial buses such as RS232, RS485, I2C and SPI bus.
2. To understand serial communication protocols.
3. To develop different applications using communications protocols.

Course Syllabus:

Unit 1: Serial Busses - Physical interface, Data and Control signals.

Unit 2: features, limitations and applications of RS232, RS485, I2 C, SPI.

Unit 3: CAN - Architecture, Data transmission, Layers, Frame formats, applications.

Unit 4: PCI e - Revisions, Configuration space, Hardware protocols, applications.

Unit 5: USB - Transfer types, enumeration, Descriptor types and contents, Device driver.

Unit 6: Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fiber optic and copper cable.

Course Outcome:

At the end of the course, students will be able to:

1. Select a particular serial bus suitable for a particular application.
2. Develop APIs for configuration, reading and writing data onto serial bus.
3. Design and develop peripherals that can be interfaced to desired serial bus.

References:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition.
2. Jan Axelson, “USB Complete”, Penram Publications.
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press.
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x.
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org.

PEC-EV-524 Network Security and Cryptography (3-0-2-4)

Course Objectives:

1. To understand the fundamentals of Cryptography.
2. To acquire knowledge on standard algorithms used to provide confidentiality, integrity and authenticity.
3. To understand the various key distribution and management schemes.
4. To understand how to deploy encryption techniques to secure data in transit across data networks.
5. To design security applications in the field of Information technology.

Course Syllabus:

Unit 1: Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit 2: Number Theory - Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3: Private-Key (Symmetric) Cryptography - Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4: Public-Key (Asymmetric) Cryptography - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 5: Authentication - IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6: System Security - Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.Security - Need, security services, Attacks, OSI Security Architecture, one time passwords.

Course Outcome:

At the end of the course, students will be able to:

1. Identify and utilize different forms of cryptography techniques.
2. Incorporate authentication and security in the network applications.
3. Distinguish among different types of threats to the system and handle the same.

References:

1. William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communication in a Public World”, Prentice Hall, 2nd Edition.
3. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Pres.
4. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “Inside Network Perimeter Security”, Pearson Education, 2nd Edition.
5. Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident.

OEC-801 Business Analytics (3-0-0-3)

Course objectives:

1. Understand the role of business analytics within an organization.
2. Analyze data using statistical and data mining techniques and understand relationships between the underlying business processes of an organization.
3. To gain an understanding of how managers use business analytics to formulate and solve business problems and to support managerial decision making.
4. To become familiar with processes needed to develop, report, and analyze business data.
5. Use decision-making tools/Operations research techniques.

Course Syllabus:

Unit 1: Business analytics: Overview of Business analytics, Scope of Business analytics, Business Analytics Process, Relationship of Business Analytics Process and organization, competitive advantages of Business Analytics. Statistical Tools: Statistical Notation, Descriptive Statistical methods, Review of probability distribution and data modeling, sampling and estimation methods overview.

Unit 2: Trendiness and Regression Analysis: Modeling Relationships and Trends in Data, simple Linear Regression. Important Resources, Business Analytics Personnel, Data and models for Business analytics, problem solving, Visualizing and Exploring Data, Business Analytics Technology.

Unit 3: Organization Structures of Business analytics, Team management, Management Issues, Designing Information Policy, Outsourcing, Ensuring Data Quality, Measuring contribution of Business analytics, Managing Changes. Descriptive Analytics, predictive analytics, predicative Modeling, Predictive analytics analysis, Data Mining, Data Mining Methodologies, Prescriptive analytics and its step in the business analytics Process, Prescriptive Modeling, nonlinear Optimization.

Unit 4: Forecasting Techniques: Qualitative and Judgmental Forecasting, Statistical Forecasting Models, Forecasting Models for Stationary Time Series, Forecasting Models for Time Series with a Linear Trend, Forecasting Time Series with Seasonality, Regression Forecasting with Casual Variables, Selecting Appropriate Forecasting Models. Monte Carlo Simulation and Risk Analysis: Monte Carle Simulation Using Analytic Solver Platform, New-Product Development Model, Newsvendor Model, Overbooking Model, Cash Budget Model.

Unit 5: Decision Analysis: Formulating Decision Problems, Decision Strategies with the without Outcome Probabilities, Decision Trees, the Value of Information, Utility and Decision Making.

Unit 6: Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data journalism.

Course Outcomes:

1. Students will demonstrate knowledge of data analytics.
2. Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
3. Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
4. Students will demonstrate the ability to translate data into clear, actionable insights.

Reference:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

OEC-802 Industrial Safety (3-0-0-3)

Course Syllabus:

Unit 1: Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

Unit 2: Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

Unit 3: Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, Screw down grease cup, Pressure grease gun, Splash lubrication, Gravity lubrication, Wick feed lubrication, Side feed lubrication, Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

Unit 4: Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, Any one machine tool, Pump, Air compressor, Internal combustion engine, Boiler, Electrical motors, Types of faults in machine tools and their general causes.

Unit 5: Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance.

Unit 6: Steps/procedure for periodic and preventive maintenance of: Machine tools, Pumps, Air compressors, Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance.

Reference:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.
3. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
4. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

OEC-803 Operations Research (3-0-0-3)

Course Syllabus:

Unit 1: Optimization Techniques, Model Formulation, models, General L.R Formulation, Simplex Techniques, Sensitivity Analysis, Inventory Control Models.

Unit 2: Formulation of a LPP - Graphical solution revised simplex method - duality theory - dual simplex method - sensitivity analysis - parametric programming.

Unit 3: Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem - max flow problem - CPM/PERT.

Unit 4: Scheduling and sequencing - single server and multiple server models - deterministic inventory models - Probabilistic inventory control models - Geometric Programming.

Unit 5: Competitive Models, Single and Multi-channel Problems, Sequencing Models, Dynamic Programming, Flow in Networks, Elementary Graph Theory, Game Theory Simulation.

Course Outcomes:

1. Students should able to apply the dynamic programming to solve problems of discreet and continuous variables.
2. Students should able to apply the concept of non-linear programming.
3. Students should able to carry out sensitivity analysis.
4. Student should able to model the real world problem and simulate it.

References:

1. H.A. Taha, Operations Research And Introduction, PHI, 2008.
2. H.M. Wagner, Principles of Operations Research, PHI, Delhi, 1982.
3. J.C. Pant, Introduction to Optimisation: Operations Research, Jain Brothers, Delhi, 2008.
4. Hitler Libermann Operations Research: McGraw Hill Pub. 2009.
5. Pannerselvam, Operations Research: Prentice Hall of India 2010.
6. Harvey M Wagner, Principles of Operations Research: Prentice Hall of India 2010.

OEC-804 Cost Management of Engineering Projects (3-0-0-3)

Course Syllabus:

Unit 1: Introduction and Overview of the Strategic Cost Management Process, Cost concepts in decision-making; relevant cost, Differential cost, Incremental cost and Opportunity cost. Objectives of a Costing System; Inventory valuation; Creation of a Database for operational control; Provision of data for Decision-Making.

Unit 2: Project: meaning, Different types, why to manage, cost overruns centers, various stages of project execution: conception to commissioning. Project execution as conglomeration of technical and nontechnical activities. Detailed Engineering activities. Pre project execution main clearances and documents Project team: Role of each member. Importance Project site: Data required with significance. Project contracts. Types and contents. Project execution Project cost control. Bar charts and Network diagram. Project commissioning: mechanical and process.

Unit 3: Cost Behavior and Profit Planning Marginal Costing; Distinction between Marginal Costing and Absorption Costing; Break-even Analysis, Cost-Volume-Profit Analysis. Various decision-making problems. Standard Costing and Variance Analysis.

Unit 4: Pricing strategies: Pareto Analysis. Target costing, Life Cycle Costing. Costing of service sector. Just-in-time approach, Material Requirement Planning, Enterprise Resource Planning, Total Quality Management and Theory of constraints.

Unit 5: Activity-Based Cost Management, Bench Marking; Balanced Score Card and Value-Chain Analysis. Budgetary Control; Flexible Budgets; Performance budgets; Zero-based budgets. Measurement of Divisional profitability pricing decisions including transfer pricing.

Unit 6: Quantitative techniques for cost management, Linear Programming, PERT/CPM, Transportation problems, Assignment problems, Simulation, Learning Curve Theory.

References:

1. Cost Accounting A Managerial Emphasis, Prentice Hall of India, New Delhi.
2. Charles T. Horngren and George Foster, Advanced Management Accounting.
3. Robert S Kaplan Anthony A. Alkinson, Management & Cost Accounting.
4. Ashish K. Bhattacharya, Principles & Practices of Cost Accounting A. H. Wheeler publisher.
5. N.D. Vohra, Quantitative Techniques in Management, Tata McGraw Hill Book Co. Ltd.

OEC-805 Composite Materials (3-0-0-3)

Course Syllabus:

Unit 1: Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

Unit 2: Reinforcements: Preparation-layup, curing, properties and applications of glass fibers, carbon fibers, Kevlar fibers and Boron fibers. Properties and applications of whiskers, particle reinforcements. Mechanical Behavior of composites: Rule of mixtures, Inverse rule of mixtures. Isostrain and Isostress conditions.

Unit 3: Manufacturing of Metal Matrix Composites: Casting – Solid State diffusion technique, Cladding – Hot isostatic pressing. Properties and applications. Manufacturing of Ceramic Matrix Composites: Liquid Metal Infiltration – Liquid phase sintering. Manufacturing of Carbon – Carbon composites: Knitting, Braiding, Weaving. Properties and applications.

Unit 4: Manufacturing of Polymer Matrix Composites: Preparation of Moulding compounds and prepregs – hand layup method – Autoclave method – Filament winding method – Compression moulding – Reaction injection moulding. Properties and applications.

Unit 5: Strength: Laminar Failure Criteria-strength ratio, maximum stress criteria, maximum strain criteria, interacting failure criteria, hygrothermal failure. Laminate first play failure-insight strength; Laminate strength-ply discount truncated maximum strain criterion; strength design using caplet plots; stress concentrations.

References:

1. Material Science and Technology – Vol 13 – Composites by R.W.Cahn – VCH, West Germany.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.
3. Hand Book of Composite Materials-ed-Lubin.
4. Composite Materials – K.K.Chawla.
5. Composite Materials Science and Applications – Deborah D.L. Chung.
6. Composite Materials Design and Applications – Danial Gay, Suong.

OEC-806 Waste to Energy (3-0-0-3)

Course Syllabus:

Unit 1: Introduction to Energy from Waste: Classification of waste as fuel: Agro based, Forest residue, Industrial waste, MSW, Conversion devices, Incinerators, gasifiers, digestors.

Unit 2: Biomass Pyrolysis: Pyrolysis: Types, slow fast, Manufacture of charcoal, Methods, Yields and application, Manufacture of pyrolytic oils and gases, yields and applications.

Unit 3: Biomass Gasification: Gasifiers, Fixed bed system, Downdraft and updraft gasifiers, Fluidized bed gasifiers, Design, construction and operation, Gasifier burner arrangement for thermal heating, Gasifier engine arrangement and electrical power Equilibrium and kinetic consideration in gasifier operation.

Unit 4: Biomass Combustion: Biomass stoves, Improved chullahs, types, some exotic designs, fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation, Operation of all the above biomass combustors.

Unit 5: Biogas: Properties of biogas (Calorific value and composition), Biogas plant technology and status, Bio energy system, Design and constructional features, Biomass resources and their classification, Biomass conversion processes.

Unit 6: Thermo chemical conversion, Direct combustion, biomass gasification, pyrolysis and liquefaction, biochemical conversion, anaerobic digestion, Types of biogas Plants, Applications, Alcohol production from biomass, Bio diesel production, Urban waste to energy conversion, Biomass energy programme in India.

References:

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
4. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.

OEC-807 Cyber Security (3-0-0-3)

Course Syllabus:

Unit 1: Cyber Security Basics – Overview, What is Cyber Security? What does it matters to us? Where do we use every day? How does it impact you? Your society? Your Country?

Unit 2: Cyber Attacks and Impact Cyber Attacks types: External, Internal, and End Point Cyber Attacks and Exploits Hackers and Hacking System Level Memory/Integer/ Operating system level attacks, Cyber Security, Protection Methods: NSA Security, Frame Work Model, Detection, Identification, and Protection Risk Mitigation.

Unit 3: Internal Security: Enterprise Internal Security, Internal Security Access Control, MFA, and SSO Operating System Level Security, Security Codes: Signatures, Sandboxes, and Patterns Detection & Isolation Security Mechanisms based on Signatures, Security Mechanisms based on Sandboxes, Security Mechanisms based on Legacy and Patterns Detection, Identification and Isolation Security Exploitation Techniques, Hackers and hacking methods, Exploiting Wireless Devices, Multiple Exploitation Mechanisms and impact on Systems.

Unit 4: Web Cyber Security Models and Challenges: NSA based Web Cyber Security Model, Frame work, Browser Security Architecture, Browser Security impact and challenges, Web Application Cyber Security Challenges, SQL Injection, attacks on the Web Servers, Web Application Security Design and Implementation – Case Study, Internal Security, Identity Access Control Management (IAM), Single Sign On (SSO), Multi Factor Authentication (MFA), Internal Data Integrity and Data protection, Security & Regulatory Compliance, HIPPA, PCI-DSS, FISMA, SOX, CDI.

Unit 5: Cryptography and Crypto Currencies: Cryptography Security Methods, Hash Keys and Security protection methods, Data Breach attacks due to internal loop holes, Crypto Currencies and Security impact – Case Study of Bit Coins.

Unit 6: Network Security: External Security Threats and Challenges, Routers, Switches, and Gateways etc, Data Traffic Irregularities and DDOS Attacks, Network Security Vulnerabilities: Ingress and Egress Traffic Security Management, Firewalls, VPN's, and Other Security Solutions, How do you protect the network? Various data breach types and network security impact assessment. Dynamic Threat Intelligence: Threat Intelligence Prediction, Risk Mitigation, Mobile Devices and Platform Security, Mobile Operating Systems & Security Overview, Android and IOS security challenges, Mobile Threats and Malware challenges.

Course outcomes

1. To master fundamentals of secret and public cryptography.
2. To master understanding external and internal threats to an organization,

3. To be familiar with network security threats and countermeasures,

References

1) Matt Bishop, " Computer Security Art and Science", Pearson/PHI, 2002.

fortify UNIX networks."
2) Corey Schou, Steven Hernandez,"Information Assurance Handbook: Effective Computer Security and Risk Management Strategies "

PRJ-EV-525 Mini Project and Seminar (0-0-4-2)

Every student will be given mini project at the start of semester. He/she has to work on the completion of the same under supervisor(s) allotted. He has to deliver two presentations during the semester immediately after Mid Semester and second at the end of semester and every student has to select the topic of seminar at the start of semester through searching of IEEE/IET/Springer/Elsevier/Other resources from latest publications in the field of VLSI and Embedded systems. He has to deliver two presentations during the semester I immediately after Mid Semester and second at the end of semester. A student has to write a review paper based on the study that he performs during the course of a semester.

AUD-902 Disaster Management (2-0-0-0)

Course Objectives:

1. Learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
2. Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
3. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
4. Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Course Syllabus:

Unit 1: Introduction Disaster: Definition, Factors and Significance; Difference between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Unit 2: Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

Unit 3: Disaster Prone Areas In India Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics.

Unit 4: Disaster Preparedness And Management Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.

Unit 5: Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Unit 6: Disaster Mitigation Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs Of Disaster Mitigation in India.

References:

1. R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company.
2. Sahni, PardeepEt.Al. (Eds.)," Disaster Mitigation Experiences and Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L. "Disaster Administration and Management Text and Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

AUD-903 Sanskrit for Technical Knowledge (2-0-0-0)

Course Objectives:

1. To get a working knowledge in illustrious Sanskrit, the scientific language in the world.
2. Learning of Sanskrit to improve brain functioning 3. Learning of Sanskrit to develop the logic in mathematics, science & other subjects enhancing the memory power.
3. The engineering scholars equipped with Sanskrit will be able to explore the huge knowledge from ancient literature.

Course Syllabus:

Unit 1: Alphabets in Sanskrit.

Unit 2: Past/Present/Future Tense.

Unit 3: Simple Sentences, Order.

Unit 4: Introduction of roots.

Unit 5: Technical information about Sanskrit Literature.

Unit 6: Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics.

Course Outcomes:

1. Understanding basic Sanskrit language.
2. Ancient Sanskrit literature about science & technology can be understood.
3. Being a logical language will help to develop logic in students.

References:

1. “Abhyaspustakam” – Dr.Vishwas, Samskrita-Bharti Publication, New Delhi.
2. “Teach Yourself Sanskrit” PrathamaDeeksha-VempatiKutumbshastri, Rashtriya Sanskrit Sansthanam, New Delhi Publication.
3. “India’s Glorious Scientific Tradition” Suresh Soni, Ocean books (P) Ltd., New Delhi.

AUD-904 Value Education (2-0-0-0)

Course Objectives:

1. Understand value of education and self- development.
2. Imbibe good values in students.
3. Should know about the importance of character.

Course Syllabus:

Unit 1: Values and self-development –Social values and individual attitudes. Work ethics, Indian vision of humanism. Moral and non- moral valuation. Standards and principles. Value judgements, Importance of cultivation of values.

Unit 2: Sense of duty. Devotion, Self-reliance. Confidence, Concentration. Truthfulness, Cleanliness. Honesty, Humanity. Power of faith, National Unity. Patriotism. Love for nature, Discipline.

Unit 3: Personality and Behavior Development - Soul and Scientific attitude. Positive Thinking. Integrity and discipline. Punctuality, Love and Kindness. Avoid fault Thinking.

Unit 4: Free from anger, Dignity of labour. Universal brotherhood and religious tolerance. True friendship. Happiness Vs suffering, love for truth. Aware of self-destructive habits.Association and Cooperation.

Unit 5: Doing best for saving natureCharacter and Competence –Holy books vs Blind faith. Self-management and Good health. Science of reincarnation.

Unit 6: Equality, Nonviolence, Humility, Role of Women. All religions and same message,Mind your Mind, Self-control. Honesty, studying effectively.

Course Outcomes:

1. Knowledge of self-development.
2. Learn the importance of Human values.
3. Developing the overall personality.

References:

1. Chakroborty, S.K. “Values and Ethics for organizations Theory and practice”, Oxford University Press, New Delhi.

AUD-905 Constitution of India (2-0-0-0)

Course Syllabus:

Unit 1: History of Making of the Indian Constitution: History Drafting Committee, (Composition & Working).

Unit 2: Philosophy of the Indian Constitution: Preamble Salient Features.

Unit 3: Contours of Constitutional Rights & Duties: Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies , Directive Principles of State Policy , Fundamental Duties.

Unit 4: Organs of Governance: Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

Unit 5: Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO of Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy (Different departments), Village level: Role of Elected and Appointed officials, Importance of grass root democracy.

Unit 6: Election Commission: Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners. State Election Commission: Role and Functioning. Institute and Bodies for the welfare of SC/ST/OBC and women.

Course Outcomes:

1. Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
2. Discuss the intellectual origins of the framework of argument that informed the conceptualization of social reforms leading to revolution in India.
3. Discuss the circumstances surrounding the foundation of the Congress Socialist Party [CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
4. Discuss the passage of the Hindu Code Bill of 1956.

References:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. Dr. S. N. Busi, Dr. B. R. Ambedkar framing of Indian Constitution, 1st Edition, 2015.
3. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.

4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AUD-906 Pedagogy Studies (2-0-0-0)

Course Objectives:

1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
2. Identify critical evidence gaps to guide the development.

Course Syllabus:

Unit 1: Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions, Overview of methodology and Searching. Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries, Curriculum, Teacher education.

Unit 2: Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies, How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?, Theory of change, Strength and nature of the body of evidence for effective pedagogical practices, Pedagogic theory and pedagogical approaches, Teachers' attitudes and beliefs and Pedagogic strategies.

Unit 3: Professional development: alignment with classroom practices and follow-up support, Peer support Support from the head teacher and the community, Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Unit 4: Research gaps and future directions, Research design, Contexts, Pedagogy, Teacher education , Curriculum and assessment , Dissemination and research impact.

Course Outcomes:

1. What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?
2. What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
3. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

References:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.

3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

AUD-907 Stress Management by ancient Indian Techniques (2-0-0-0)

Course Objectives:

1. To achieve overall health of body and mind.
2. To overcome stress.

Course Syllabus:

Unit 1: Definitions of Eight parts of yog. (Ashtanga), Yam and Niyam. Do`s and Don't's in life.

Unit 2: Ahinsa, satya, astheya, bramhacharya and aparigraha, Shaucha, Santosh, tapa, swadhyay, ishwarpranidhan.

Unit 3: Asan and Pranayami) Various yog poses and their benefits for mind & body.

Unit 4: Regularization of breathing techniques and its effects-Types of pranayama.

Course Outcomes:

Students will be able to:

1. Develop healthy mind in a healthy body thus improving social health.
2. Also Improve efficiency.

References:

1. "Yogic Asanas for Group Tarining-Part-I" :Janardan Swami YogabhyasiMandal, Nagpur.
2. "Rajayoga or conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata.

AUD-908 Personality Development through Life Enlightenment Skills (2-0-0-0)

Course Objectives:

1. To learn to achieve the highest goal happily.
2. To become a person with stable mind, pleasing personality and determination.
3. To awaken wisdom in students.

Course Syllabus:

Unit 1: Neeti satakam-Holistic development of personality.

Unit 2: Approach to day to day work and duties.

Unit 3: Statements of basic knowledge, Personality of Role model.

Course Outcomes:

Students will be able to

1. Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life.

2. The person who has studied Geeta will lead the nation and mankind to peace and prosperity.

3. Study of Neetishatakam will help in developing versatile personality of students.

References:

1. "Srimad Bhagavad Gita" by Swami SwarupanandaAdvaita Ashram (Publication Department), Kolkata.
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.

DIS-EV-601 Dissertation Phase-I (0-0-28-14)

Dissertation shall consist of: Research work done by the candidate in the areas related to the chosen specialization, or Comprehensive and critical review of any recent development in the chosen specialization, or Design and/or development of a product related to the program done by the candidate.

Following shall be the guidelines for evaluation of dissertation phase-I

- Dissertation Phase-I shall consist of the following components (whichever applicable) Extensive literature survey, Data collection from R&D organizations, Industries, etc. Study of the viability, applicability and scope of the dissertation Detailed Design (H/W and S/W as applicable), Partial implementation.
- A candidate should prepare the following documents for examination:
- A term paper in the format of any standard journal based on the work.
- A detailed report of the work done by the candidate related to dissertation.
- Every candidate should present himself (for about 30 min.) before the panel of examiners (which will evaluate the dissertation phase-I for TW and Oral marks) consisting of Head of Department, M. Tech. Coordinator or his nominee, all supervisors.

DIS-EV-602 Dissertation Phase-II (0-0-28-14)

The dissertation shall be assessed internally by a panel of examiners (similar to the one in dissertation phase- I) before submission. The candidate shall submit the dissertation in triplicate to the Head of the institution, duly certified that the work has been satisfactorily completed. The Practical examination (viva-voce) shall consist of a defense presented by the candidate or his/her work in the presence of examiners appointed by the University one of whom will be the supervisor and the other an external examiner.